IN THE CLAIMS

Please amend the claims as follows:

1. (cancelled)

2. (cancelled)

3. (cancelled)

4. (cancelled)

5. (cancelled)

6. (cancelled)

7 (cancelled)

8 (cancelled)

9 (cancelled)

10. (currently amended) ~~The apparatus of claim 2~~ An apparatus for self-initiated instruction issuing comprising:

an instruction queue operable for issuing at least one instruction to an execution unit, said queue including a plurality of entries, each queue entry having a first portion and a second portion, said first portion operable for storing a first link data value and said second portion operable for storing a first data value, said first portion comprising a link mask and said first link data value indicating a target instruction which of the queue's plurality of entries that a dispatching dependent instruction will occupy, wherein said first data value in a first queue entry is set in response to a first link data value in a preselected second queue entry, wherein at least one instruction is selected for issuing in response to a predetermined first data value in a corresponding queue entry;

a rename register device coupled to said queue, said rename register device including a plurality of entries, each entry having a first portion operable for storing a pointer data value and a second portion operable for storing a validity data value, wherein each said pointer data value is associated with a corresponding queue entry, wherein each said first link data value is set in response to said pointer data values and said validity data values, wherein each said rename register device entry includes a third portion

operable for receiving a plurality of operand tags, and wherein each said pointer data value is operable for selection in response to a preselected one of said plurality of operand tags, wherein each said queue entry includes a third portion coupled to said rename register device for receiving a first one of said plurality of operand tags, and a fourth portion coupled to said rename register device for receiving a second one of said plurality of operand tags, wherein said first and second operand tags are associated with a dispatching instruction, and wherein said first operand tag is further associated with said first link data value, wherein said queue is operable for broadcasting a preselected first operand tag; and

a storage device operable for receiving said broadcasting of said first operand tag, wherein each said rename register device entry ~~includes a~~ includes a fourth portion operable for storing a second data value, said second data value being operable for setting in response to an issuing instruction.

11. (original) The apparatus of claim 10 wherein said first data value is operable for setting in response to said second data value.

12. (currently amended) The apparatus of claim [[4]] 10 each said queue entry further comprises a fifth portion operable for storing a second link data value and a sixth portion operable for storing a second data value, and a seventh portion coupled to said rename register device for receiving a third one of said plurality of operand tags, said third operand tag being associated with said dispatching instruction, and wherein said third operand tag is further associated with said second link data value, and wherein said second data value in said first queue entry is set in response to a preselected second link data value in a third queue entry.

13. (original) The apparatus of claim 12 wherein each said second link data value is set in response to said pointer data values and said validity data values.

14. (currently amended) A method of self-initiated instruction issuing comprising the steps of: setting a predetermined data value in a first portion of a preselected first queue entry in a queue operable for storing a plurality of instructions for issuing to an execution unit, said queue including a plurality of entries, each entry being associated with an instruction for issuing, wherein said first queue entry is preselected in response to a first data value in a second portion of a preselected second queue entry, wherein the first portion comprises a link mask and a first link data value indicating to a target instruction which of the queue's plurality of entries that a dispatching dependent instruction will occupy; and
selecting for issuing an instruction associated with said entry containing said predetermined data value in said first portion in response to said predetermined data value.

15. (original) The method of claim 14 further comprising the step of, if said dispatching instruction is a one-cycle piped instruction, storing a first queue pointer data value associated with said dispatching instruction in a first portion of an associated rename register entry, said rename register including a plurality of entries, wherein said queue pointer value associates said rename register entry and said preselected queue entry corresponding to said dispatching instruction, and wherein said second queue entry is selected in response to a second queue pointer value.

16. (original) The method of claim 14 further comprising the step of setting said first data value in response to a source operand data value of said dispatching instruction.

17. (original) The method of claim 15 wherein said step of setting said first data value is omitted in response to a predetermined data value in said first portion of said rename register entry.

18. (cancelled)

19. (original) The method of claim 14 wherein said step of setting said predetermined data value in said first portion is in response to an issuing of an instruction associated with said second queue entry.

20. (cancelled)

21. (cancelled)

22. (cancelled)

23. (cancelled)

24. (cancelled)

25. (original) The method of claim 15 wherein said second queue pointer value is associated with a source operand tag of said dispatching instruction.

26. (original) The method of claim 25 wherein said second queue pointer value corresponds two to a queue entry of an instruction target operand tag matching said source operand.

27. (original) The method of claim 14 wherein said first data value comprises a link mask having a number of bits equal to a number of entries in said queue.

28. (original) The method of claim 14 wherein said step of setting said predetermined data value is in response to an issuing of an instruction associated with said second queue entry.

29. (currently amended) A data processing system for self-initiated instruction issuing comprising:

an input means for communicating a plurality of instructions;

a dispatch unit coupled to said input means;

at least one execution unit coupled to said dispatch unit for receiving instructions communicated therefrom, each execution unit including a self-initiated instruction issue mechanism for receiving said instructions and issuing instructions to an execution logic circuit for execution, said self-initiated issue mechanism comprising:

an instruction queue operable for issuing at least one instruction to said execution unit, said queue including a plurality of entries, each queue entry having a first portion and a second portion, said first portion operable for storing a first link data value, said first portion comprising a link mask and said first link data value indicating to a target instruction which of the queue's plurality of entries that a dispatching dependent instruction will occupy, and said second portion operable for storing a first data value, and wherein said first data value in a first queue entry is set in response to a first link data value in a preselected second queue entry; and

a rename register device coupled to said queue, said rename register device including a plurality of entries, each entry having a first portion operable for storing a pointer data value and a second portion operable for storing a validity data value, wherein each pointer data value is associated with a corresponding queue entry, and wherein each first link data value is set in response to said pointer data values and said validity data values.

30. (original) The data processing system of claim 29 wherein each said rename register device entry includes a third portion operable for receiving a plurality of operand tags, and wherein each said pointer data value is operable for selection in response to a preselected one of said plurality of operand tags.

31. (original) The data processing system of claim 30 wherein said queue is operable for broadcasting a preselected first operand tag.

32. (original) The data processing system of claim 31 further comprising a storage device operable for receiving said broadcast first operand tag.

33. (original) The data processing system of claim 32 wherein said storage device is coupled to said rename register device, and wherein each said rename register device entry includes a fourth portion operable for storing a second data value, said second data value being operable for setting in response to said broadcast first operand tag.

34. (original) The data processing system of claim 33 wherein said first data value is operable for setting in response to said second data value.

35. (cancelled)

36. (cancelled)

37. (cancelled)

38. (currently amended) An apparatus for self-initiated processor instruction issuing including an issue queue, said issue queue comprising a plurality of entries, each entry of said plurality operable for containing information associated with an instruction to be issued, wherein each entry includes a first portion for storing an instruction operand and a second portion for storing a link value, wherein the second portion comprises a link mask and the link value indicates to a target instruction which of the issue queue's plurality of entries that a dispatching dependent instruction will occupy, and wherein, for an instruction corresponding to a first entry having a value of said instruction operand determined by an instruction corresponding to a second entry, said link value in said second entry comprises a value corresponding to a number of said first entry.

39. (previously presented) The apparatus of claim 38 wherein, for said first entry comprising an "*i*th" entry of said plurality of entries, said value representing said first entry is a value of an "*i*th" bit of a plurality of bits of said link value in said second entry.

40. (previously presented)The apparatus of claim 38 wherein each entry of said instruction queue further includes a third portion, and wherein said third portion in said first entry is operable for receiving said link value in said second entry in response to an issuing of said instruction corresponding to said second entry.

41. (previously presented)The apparatus of claim 40 wherein a data value in said third portion is operable for signaling an operand in a second portion of a corresponding entry of said plurality of entries is ready.

42. (previously presented) The apparatus of claim 38 further comprising a rename register unit coupled to said issue queue, said rename unit including a plurality of entries, said plurality of entries of said rename unit having a same number of entries as a number of entries of said instruction queue, and wherein each entry has a first portion operable for storing a data value signaling instruction information is stored in an associated entry of said plurality of entries in said issue queue.

43. (previously presented) The apparatus of claim 42 wherein each entry of said plurality of entries of said rename unit further includes a second portion operable for storing a pointer to said associated entry of said plurality of entries in said issue queue.

44. (previously presented) The apparatus of claim 38 wherein said instruction corresponding to said second entry comprises a one-cycle piped instruction.

45. (previously presented) A method for instruction issuing comprising the steps of:

setting a predetermined value in a first portion of an entry in an instruction queue corresponding to a first instruction in response to a dispatch of a second instruction; and

writing said predetermined value in a second portion of an entry in said instruction queue corresponding to said second instruction in response to an issuing of said first instruction, wherein a target of said first instruction comprises a source operand of said second instruction.

46. (previously presented) The method of claim 45 wherein said predetermined value in said first portion of said instruction queue entry is set in response to a validity value corresponding to said source operand, said validity value stored in an entry in a rename unit coupled to said instruction queue.

47. (previously presented) The method of claim 45 wherein said first instruction is a one-cycle piped instruction.

48. (currently amended) A data processing system for self-initiated instruction issuing comprising:

an instruction storage unit;

a dispatch unit coupled to said instruction storage unit;

at least one execution unit coupled to said dispatch unit for receiving instructions therefrom, each execution unit including an apparatus for issuing instructions for execution, said apparatus operable for receiving instructions from said dispatch unit, the apparatus for issuing instructions comprising an issue queue, said issue queue including a plurality of entries, each entry of said plurality operable for containing information associated with an instruction to be issued, wherein each entry includes a first portion for storing an instruction operand and a second portion for storing a link value, wherein the second portion comprises a link mask and the link value indicates to a target instruction which of the issue queue's plurality of entries that a dispatching dependent instruction will occupy, and wherein, for an instruction corresponding to a first entry having a value of said instruction operand determined by an instruction corresponding to a second entry, said link value in said second entry comprises a value representing said first entry.

49. (previously presented) The system of claim 48 wherein, for said first entry comprising an "*i*th" entry of said plurality of entries, said value representing said first entry is a predetermined value of an "*i*th" bit of a plurality of bits of said link value in said second entry.

50. (previously presented) The apparatus of claim 48 further comprising a rename register unit coupled to said issue queue, said rename unit including a plurality of entries, said plurality of entries of said rename unit having a same number of entries as a number of entries of said instruction queue, and wherein each entry has a first portion operable for storing a data value signaling instruction information is stored in an associated entry of said plurality of entries in said issue queue.

51. (previously presented) The apparatus of claim 50 wherein each entry of said instruction queue further includes a third portion, and wherein said third portion in said first entry is operable for receiving said link value in said second entry in response to an issuing of said instruction corresponding to said second entry.

52. (previously presented) The apparatus of claim 49 wherein said instruction corresponding to said second entry comprises a one-cycle piped instruction.